Quantum Confinement Controlled Positive to Negative Schottky Barrier Conversion in Ultrathin In_2O_3 Transistor Contacts

Jian-Yu Lin[1, †], Chang Niu[1, †], Zehao Lin[1], Taehyun Kim[2], Beomjin Park[2], Hyeongjun Jang[2], Changwook Jeong[2], Peide D. Ye[1, *]
[1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA
[2]Ulsan National Institute of Science and Technology, Ulsan, South Korea
[†]equal contribution, *Email: yep@purdue.edu

***Abstract* —** In this work, we study the quantum confinement (QC) effect on the Schottky barrier height (Φ_{SB}) of various metals on atomically thin In_2O_3 channels for the first time. A positive-to-negative Φ_{SB} conversion is experimentally observed by increasing the In_2O_3 channel thickness (T_{ch}) from 1.2 to 1.6 nm and above, which can be understood by QC and Fermi-level pinning (FLP) effects. To support the above understanding, FLP in metal/In_2O_3 contacts is also investigated for the first time by extracting the Φ_{SB} and pinning factor S. The close-to-zero S parameters between 0.024 – 0.004 verify the strong FLP at the metal/In_2O_3 interfaces. The contact with negative Φ_{SB} highlights the uniqueness of In_2O_3 versus other conventional semiconductors, such as Si, Ge, and monolayer MoS_2, whose Fermi-level are pinned with positive Φ_{SB}.

I. Introduction

Oxide semiconductor (OS) channel field-effect transistors (FETs) have attracted revitalized interest in recent years for their application as back-end-of-line (BEOL) compatible transistors in monolithic 3D integration, a promising technology to achieve more Moore and more than Moore [1-8]. Among various OS FETs, atomic-layer-deposited (ALD) In_2O_3 FETs have demonstrated great potential with their good conformality and uniformity on 3D structure by ALD process [2], high electron mobility of 152 $cm^2/V{\cdot}s$ [3], high on-current near 20 mA/μm in gate-all-around structure [4], ultrahigh reliability [5], and ultralow contact resistance (R_C) of 23.4 Ω·μm (measured at 10 K) approaching the quantum limit of metal/semiconductor contacts [6-7].

The recent R_C studies of In_2O_3 transistors have revealed the existence of negative Φ_{SB} contact [6-8], contrary to the positive Φ_{SB} in most of the semiconductor materials like Si [9], Ge [9], and monolayer MoS_2 [10] (as illustrated in **Fig. 1 (a)**). The negative Φ_{SB} in In_2O_3 FETs is the key reason behind the ultralow R_C approaching the quantum limit [6,7]. Therefore, it is of great importance to understand what factors affect and contribute to the negative Φ_{SB}. Under this context, this work offers the first investigation of the QC effect on the Φ_{SB} in ultrathin In_2O_3 transistors with different T_{ch}. By increasing the T_{ch} from 1.2 to ≥ 1.6 nm, the Φ_{SB} in In_2O_3 FETs can be tuned from a positive to negative value, which can be explained by a model combining the concepts of band alignment, QC, and FLP. Then, the strong FLP at the metal/In_2O_3 interface is also verified for the first time by studying the In_2O_3 FETs with various metals as contact and extracting the close-to-zero S parameters of 0.024 – 0.004 at the metal/In_2O_3 interface. **Fig. 1 (b)** summarizes the highlights of this work.

II. Experiments

Fig. 2 shows the schematic device structure of a buried-gated In_2O_3 transistor and the fabrication process flow of the devices. As the first step, 6 nm Al_2O_3 was grown by ALD on SiO_2/Si substrate as the adhesion layer of the 60 nm e-beam evaporated Ni buried gate. 4 nm HfO_2 was then deposited by ALD at 200 °C to serve as gate dielectric. Ultrathin In_2O_3 with T_{ch} between 1.2 to 2 nm was used as channel material and grown by ALD at 225 °C. Next, various metal materials were e-beam evaporated or sputtered as the source/drain (S/D) of the devices. A list of five different S/D metals used in this work and their metal work functions (Φ_M) are illustrated in **Fig. 2 (b)**. Isolation of the In_2O_3 channels was performed by inductively coupled plasma (ICP) etching. O_2 annealing at 290 °C for 10 minutes was used as an optional step for some In_2O_3 transistors.

III. Results and Discussion

A. Quantum Confinement in In_2O_3 FETs

Fig. 3 (a) presents the transfer characteristics of 1 μm long channel length (L_{ch}) In_2O_3 FETs with different T_{ch} = 1.2 – 2 nm and Pt as S/D contacts. **Fig. 4** shows the corresponding output characteristics of the same devices. As the T_{ch} increases, a negative shift of threshold voltage (V_T) and an elevation of drain current can be observed. **Fig. 3 (b)** exhibits the T_{ch}-dependent field-effect mobility (μ_{FE}) calculated from the transconductance (g_m) of L_{ch} = 1 μm devices at V_{DS} = 0.05 V. Measured gate oxide capacitance (C_{OX}) of 1.9×10^{-6} F/cm^2 for 4 nm HfO_2 was used for the μ_{FE} extraction. It should be emphasized that the extracted μ_{FE} do not exclude the effect of contact resistance (R_C) and thus are underestimated values. The μ_{FE} rises with T_{ch} and reaches a high mobility of 62 $cm^2/V{\cdot}S$ at T_{ch} = 2 nm for Pt contacts, which contributes to the good maximum drain current (I_{max}) of 720 μA/μm in **Fig. 4 (d)**. The T_{ch}-dependent properties in In_2O_3 transistors can be understood by the change of trap neutrality level (TNL) and charge neutrality level (CNL) band alignment governed by the QC effect [11]. TNL and CNL are the branch point energies where donor-like trap density and acceptor-like trap density become the same. TNL and CNL are almost the same except that TNL describes the "dielectric" and semiconductor interface while CNL characterizes the "metal" and semiconductor interface, as illustrated in **Fig. 5**. When the thickness of In_2O_3 decreases, the band alignment between TNL/CNL and conduction band minimum (E_C) will be altered by the QC effect, as demonstrated in the Density-functional-theory (DFT) simulations (**Fig. 6**). To elaborate, when the T_{ch} of the ultrathin In_2O_3 reduces, the QC will enhance the bandgap (E_g) of In_2O_3 and move the absolute energy level of E_C upwards, as shown in **Fig. 6**. In the meantime, since TNL and CNL are the intrinsic properties of the material, their absolute energy levels remain the same [11-12]. For bulk In_2O_3, it is known that the locations of TNL and CNL are ~0.4 eV above E_C (**Fig. 6 (f)**) [12-13]. As the In_2O_3 becomes thinner, the upshifting E_C will make TNL and CNL band alignments change from above E_C to below E_C (from **Fig. 6 (c)** to **(b)**) [11]. Because the location of Fermi-level (E_F) is close to TNL and CNL [11, 14], the change of these energy level alignments also impacts the carrier (i.e. electron) concentration in In_2O_3. For example, from 1.7 nm to 1.2 nm In_2O_3 films, the TNL, CNL, and E_F move from above E_C to below E_C (from **Fig. 6 (c)** to **(b)**), which indicates the transition from degenerated (higher carrier concentration) semiconductor to non-degenerated (lower carrier concentration) one. The higher carrier concentration explains why thicker In_2O_3 FETs have larger drain current compared with thinner In_2O_3 devices, as shown in **Fig. 3 (a)** and **Fig. 4**. The reduced mobility in thinner (e.g. 1.2 nm) In_2O_3 films, as presented in **Fig. 3 (b)**, is due to the increase of

surface scattering [7, 11] or the percolation conduction in atomically thin films [15].

B. Negative Schottky Barrier and Quantum Confinement

Fig. 7 presents the transfer length method (TLM) results on 1.2 and 2 nm In_2O_3 transistors to study the QC effect on R_C. The sheet resistance (R_{sh}) and R_C extracted from TLM are summarized in **Fig. 8 (a)** and **(b)**. **Fig. 8 (a)** shows that the R_{sh} decreases as the In_2O_3 channel becomes thicker, which agrees well with the larger μ_{FE} in thicker In_2O_3. On the other hand, in **Fig. 8 (b)**, the R_C demonstrates a 90 % decrease from 3285 to 319 Ω·μm at $V_{GS} - V_T = 2$ V when the T_{ch} increases from 1.2 to 2 nm. The large R_C in 1.2 nm In_2O_3 FETs with Pt as S/D contact limits the g_m scaling with L_{ch}, as shown in **Fig. 8 (c)**. To find out the reason behind the T_{ch}-dependent R_C, temperature-dependent I_D–V_{GS} curves were measured to analyze the Φ_{SB} of In_2O_3 FETs with different T_{ch}, as shown in **Fig. 9**. **Fig. 10** plots the Arrhenius plots, ln ($I_D/T^{1.5}$) versus 1000/T, extracted from **Fig. 9**. Based on the inset formula in **Fig. 10 (a)**, effective barrier height (Φ_B) among the In_2O_3 channel can be calculated from the slope of the linear fitting lines in the Arrhenius plots. The V_{GS}-dependent Φ_B from 1.2 to 2 nm In_2O_3 FETs are plotted in **Fig. 11 (a)**. The Φ_{SB} of the contact is defined as the Φ_B at flat band voltage, which can be identified as the gate voltage when the Φ_B stops depending linearly on V_{GS} [16]. **Fig. 11 (b)** summarizes the extracted Φ_{SB} from $T_{ch} = 1.2 – 2$ nm. As the T_{ch} becomes thick enough (from 1.2 nm to ≥ 1.6 nm), a positive to negative Φ_{SB} conversion can be observed in In_2O_3 transistors with Pt as S/D. People might wonder why it is possible to have negative Φ_{SB} in n-type In_2O_3 MOSFETs. Indeed, based on the ideal band alignment between metal/In_2O_3 and the Schottky-Mott rule (without considering the effect of CNL, as depicted in **Fig. 12 (a)**), the Φ_{SB} at the metal/In_2O_3 interface should be positive unless using a small work function metal as the contact [17]. This apparently cannot explain the observed negative Φ_{SB} at the high work-function metal Pt/In_2O_3 contact when the $T_{ch} \geq 1.6$ nm.

The negative Φ_{SB} in In_2O_3 transistors can be understood by considering the interface dipole induced by the CNL at the metal/In_2O_3 interface. **Fig. 12 (b)** and **(c)** illustrate the idea of interface dipole and how it contributes to the negative Φ_{SB} in two steps. Step 1 (**Fig. 12 (b)**): suppose the E_F is below CNL at the beginning (CNL above E_C is used for example), the empty donor-like interface traps will be positively charged (represented by red circles), creating an interface dipole. Step 2 (**Fig. 12 (c)**): to balance these positive interface charges, negative space charges (represented by blue circles) will accumulate at the In_2O_3 interface and bend down the E_C, which further brings metal Fermi-level (E_{Fm}) and In_2O_3 E_F closer to CNL. How close the E_F and CNL are will be proportional to the number of interface traps at the metal/In_2O_3 interface. If there are enormous interface traps, E_F at the interface will be strongly pinned near the energy level of CNL, which is understood as the Fermi-level pinning (FLP) effect [18]. Under the strong FLP condition, there will be a negative Φ_{SB} when the CNL is above E_C (like the 1.6 to 2 nm In_2O_3 in **Fig. 11 (b)** and **Fig. 6 (c-d)**). In contrast, there will be a positive Φ_{SB} if the CNL is under E_C (like the 1.2 nm In_2O_3 in **Fig. 11 (b)** and **Fig. 6 (b)**). Whether the CNL is above or under E_C can be modulated by QC as shown in **Fig. 6**.

C. Negative Schottky Barrier and Fermi-level Pinning

Next, FLP in In_2O_3 FETs is studied for the first time by changing the S/D metals and extracting their Φ_{SB}. **Fig. 13** shows the V_{GS}-dependent Φ_B of In_2O_3 FETs with T_{ch} = 1.2, 2 nm, and various metal contacts, such as Ti, Ni, Pd, and Pt. Φ_{SB} extracted from different T_{ch} and metals are summarized as a function of Φ_M in **Fig. 14 (a)**. It should be noted that as the T_{ch} increases from 1.2 to ≥ 1.6 nm, all the S/D metals demonstrate transitions from positive to negative Φ_{SB}. Even Pt, which has a large Φ_M and usually results in positive Schottky barrier contact in nFETs [9, 19], can form negative Φ_{SB} with $T_{ch} \geq 1.6$ nm of In_2O_3. The negative Φ_{SB} makes low R_C possible (**Fig. 8 (b)**). **Fig. 14 (b)** plots the S parameters, which can quantify the FLP effect [20], on different T_{ch}. The close-to-zero values of the S parameters from 0.024 to 0.004 corroborate the strong FLP at metal/In_2O_3 interface and support our model for the origin of negative Φ_{SB} (as discussed in **III-*B***).

D. Oxygen Annealing Effect on Negative Schottky Barrier

O_2 annealing has been adopted frequently to improve the device performance, such as subthreshold swing (SS), mobility, and reliability of In_2O_3 devices [5, 21]. Therefore, the effect of annealing on the negative Φ_{SB} is also of interest. **Fig. 15** demonstrates how O_2 annealing changes the transfer characteristics and the linearly extrapolated V_T. The annealing process shifts V_T positively by reducing the oxygen vacancies in In_2O_3 [21]. Meanwhile, the R_{sh} and R_C both increase slightly after O_2 annealing, as shown in **Fig. 16**. **Fig. 17** plots the extracted Φ_{SB} and shows that the negative Φ_{SB} can still be preserved after O_2 annealing. The less negative Φ_{SB} in annealed In_2O_3 devices can be explained by the weaker CNL interface dipole effect because of the reduced interface traps at the metal/In_2O_3 interface after O_2 annealing [21]. Note that the methodology applied here to determine the absolute values of Φ_{SB} is based on positive Schottky barrier assumption [16]. The negative values of Φ_{SB} obtained are just for a good reference and qualitative presentation. With the negative Φ_{SB}, low R_C, and O_2 annealing, current on/off ratio (I_{on}/I_{off}) > 10^8 (**Fig. 18 (a)**) and maximum drain current (I_{max}) around 4.5 mA/μm (**Fig. 18 (b)**) can be achieved in a 40 nm short channel In_2O_3 FET at 33K.

IV. Conclusion

For the first time, this research investigates the QC effect on Φ_{SB} in ultrathin In_2O_3 transistor contacts with different T_{ch}. By controlling the T_{ch} of In_2O_3 transistors from 1.2 to 2 nm, a positive-to-negative conversion of Φ_{SB} is observed and explained by a model combining band-alignment, QC, and FLP effects. To validate the above model, the FLP in In_2O_3 FETs is studied for the first time by extracting the Φ_{SB} from device contacts with different metals. Extracted S parameters from 0.024 to 0.004 of different T_{ch} In_2O_3 indicate the strong FLP at the metal/In_2O_3 interface. **Fig. 19** shows the benchmark of FLP studies on n-Si [9], n-Ge [9], monolayer MoS_2 [10], and ultrathin In_2O_3 (this work: $T_{ch} = 1.6 – 2$ nm). In great contrast to n-Si, n-Ge, and monolayer MoS_2 with pinned positive Φ_{SB}, ultrathin In_2O_3 makes itself so unique by having pinned negative Φ_{SB}.

Acknowledgment: The work is supported by SRC and Samsung Electronics.

References: [1] S. Datta *et al.*, *IEEE Micro*, pp. 8, 2019. [2] M. Si *et al.*, *IEEE-TED*, p. 6605, 2021. [3] Z. Lin *et al., 2024 VLSI*, T4-3. [4] Z. Zhang *et al.*, *IEEE-EDL*, p. 1905, 2022. [5] Z. Zhang *et al., 2023 VLSI*, T11-3. [6] C. Niu *et al., 2023 IEDM*, 37-2. [7] C. Niu *et al., IEEE-TED*, pp. 3403, 2024. [8] S. Lee *et al., 2024 VLSI*, T16-3. [9] T. Nishimura *et al., Appl. Phys. Lett., p. 123123,* 2007. [10] C. Kim *et al.*, *ACS Nano*, p. 1588, 2017. [11] M. Si *et al.*, *Nano Letters*, pp. 500, 2021. [12] Van de Walle *et al.*, *Nature*, p. 626–628, 2003. [13] P. D. C. King *et al.*, *Phys. Rev. Lett.*, p. 116808, 2008. [14] P. D. Ye, *J. Vac. Sci. Technol. A*, p. 697, 2008. [15] S. Lee *et al.*, *Appl. Phys. Lett.*, p. 203508, 2011. [16] Allain, A. *et al.*, *Nature Mater*, p.1195, 2015. [17] W. Schottky, *Z. Phys.*, p. 367, 1939. [18] A. M. Cowley, S. M. Sze, *J. Appl. Phys.,* p. 3212, 1965. [19] L. Jiao *et al.*, *2023 IEDM*, 24-6. [20] R. T. Tung, *Appl. Phys. Rev.*, p. 011304, 2014. [21] M. Si *et al.*, *IEEE-TED*, pp. 1075, 2021. [22] H. Kawano, *Progress in Surface Science*, Pages 1-165, 2008. [23] Søren Smidstrup *et al*, *J. Phys.: Condens. Matter*, p. 015901, 2020.

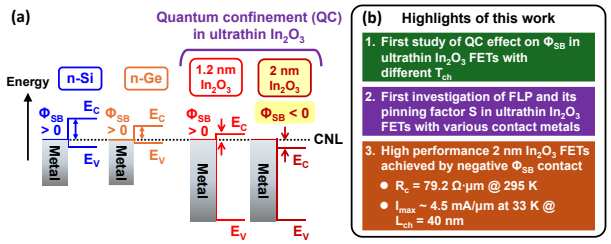

Fig. 1. (a) Overview of the Fermi-level pinning (FLP) in different semiconductors. **(b)** Highlights of this work.

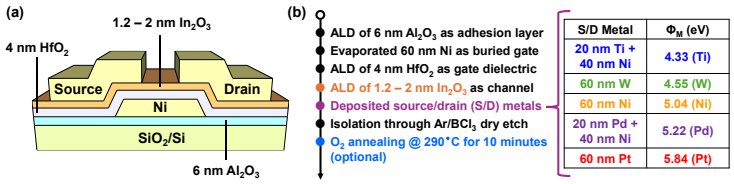

Fig. 2. (a) Device schematic of a buried-gated In_2O_3 transistor. **(b)** Fabrication process flow of buried-gated In_2O_3 transistors with five different S/D metal contacts. The Φ_M of the metals used in this work can be found in [22].

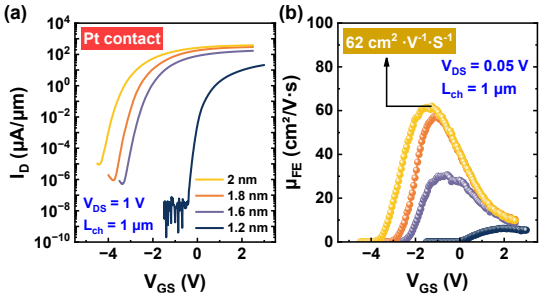

Fig. 3. (a) Transfer characteristics of In_2O_3 FETs with Pt as S/D contact, L_{ch} = 1 μm, and T_{ch} = 1.2, 1.6, 1.8, and 2 nm. **(b)** Extracted μ_{FE} from the g_m of In_2O_3 FETs with different T_{ch}.

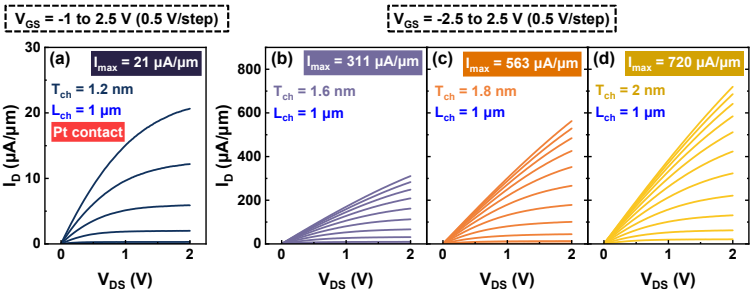

Fig. 4. Output characteristics of In_2O_3 FETs with Pt as S/D metal contact, L_{ch} = 1 μm, and different T_{ch} of **(a)** 1.2, **(b)** 1.6, **(c)** 1.8, and **(d)** 2 nm. A high maximum drain current (I_{max}) = 720 μA/μm can be reached in the T_{ch} = 2 nm device.

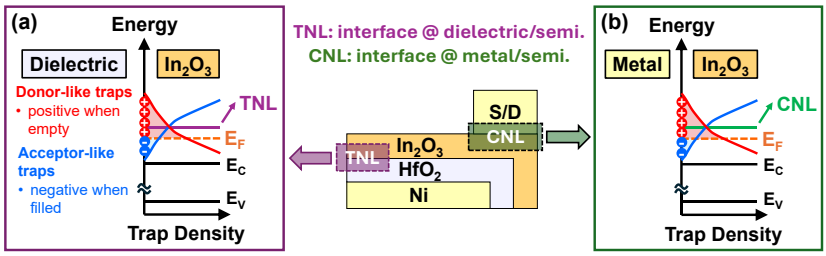

Fig. 5. Schematic trap density distribution at the interfaces between **(a)** gate dielectric (HfO_2) and semiconductor (In_2O_3); **(b)** metal (S/D contact) and semiconductor (In_2O_3). TNL describes the dielectric/semiconductor interface while CNL characterizes the metal/semiconductor interface. The absolute energy levels of TNL and CNL are expected to be similar [11].

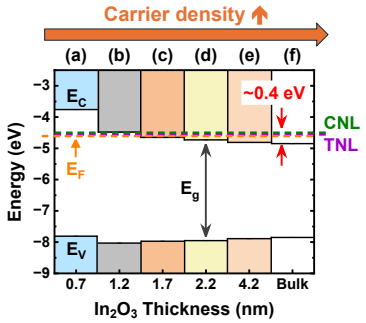

Fig. 6. DFT simulation results of the band alignments in In_2O_3 films with different T_{ch} of **(a)** 0.7 nm, **(b)** 1.2 nm, **(c)** 1.7 nm, **(d)** 2.2 nm, **(e)** 4.2 nm, and **(f)** bulk. QuantumATK was used for DFT simulations [23].

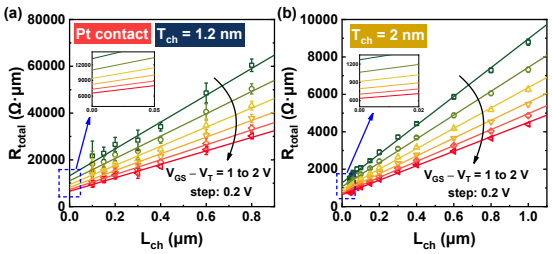

Fig. 7. TLM measurements on **(a)** 1.2 nm and **(b)** 2 nm In_2O_3 devices with Pt S/D contacts.

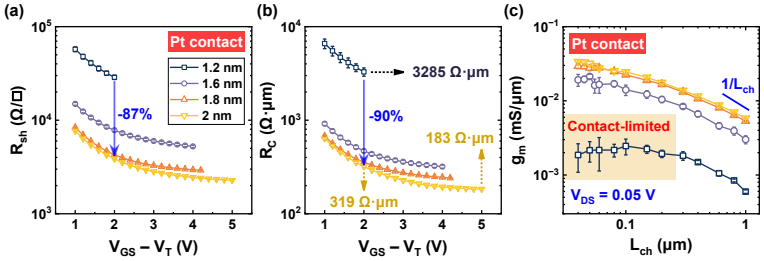

Fig. 8. Extracted **(a)** R_{sh} and **(b)** R_C as a function of V_{GS}–V_T in In_2O_3 transistors with Pt contact and various T_{ch}. **(c)** g_m extracted from I_D – V_{GS} curves as a function of L_{ch}.

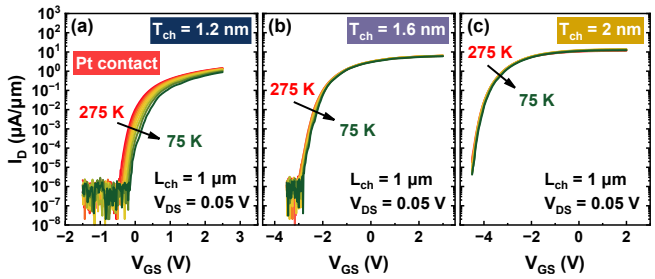

Fig. 9. Temperature-dependent transfer characteristics of In_2O_3 FETs with Pt contact, L_{ch} = 1 μm, V_{DS} = 0.05 V, and T_{ch} of **(a)** 1.2, **(b)** 1.6, and **(c)** 2 nm.

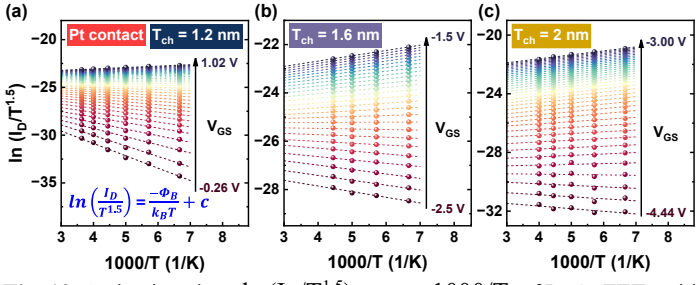

Fig. 10. Arrhenius plots, ln ($I_D/T^{1.5}$) versus 1000/T, of In_2O_3 FETs with T_{ch} of **(a)** 1.2, **(b)** 1.6, and **(c)** 2 nm at different V_{GS} are extracted from **Fig. 9**. Dash lines represent the linear fitting of the data.

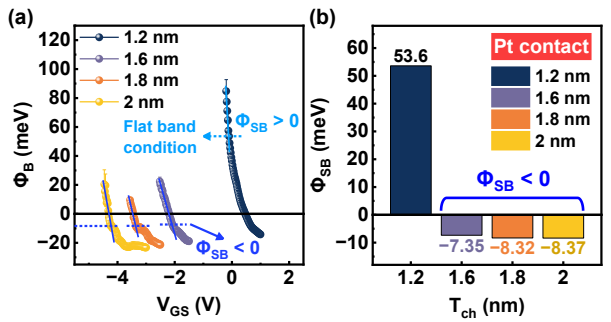

Fig. 11. (a) V_{GS}–dependent channel barrier height (Φ_B) extracted from the slope of the linear fitting lines in the Arrhenius plots like **Fig. 10**. The Φ_B at flat band voltage is the Schottky Barrier height (Φ_{SB}) of contact. **(b)** Extracted Φ_{SB} from In_2O_3 FETs with different T_{ch}.

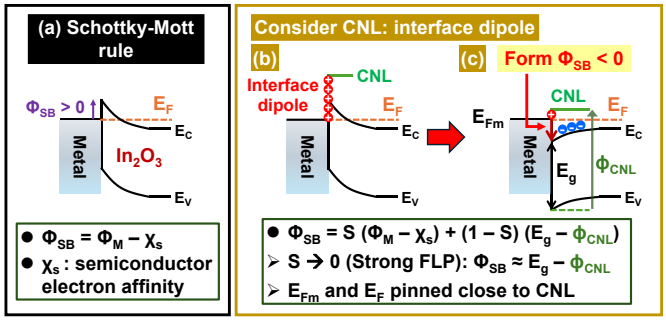

Fig. 12. (a) Illustration of Schottky-Mott rule (S = 1): assumes no FLP at metal/semiconductor (In_2O_3) interface. **(b)** Real situation (S < 1): needs to consider the interface dipole effect induced by CNL, which is the key to achieving $\Phi_{SB} < 0$ and the cause of FLP.

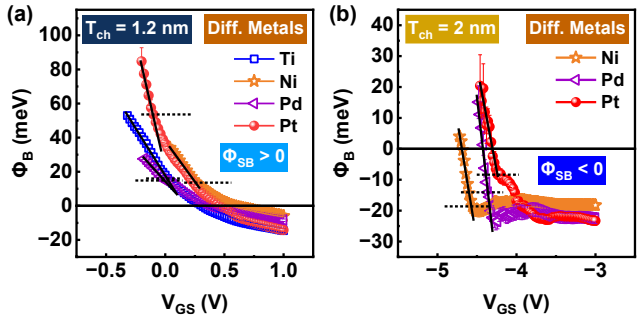

Fig. 13. V_{GS} – dependent Φ_B extracted from In_2O_3 FETs with **(a)** T_{ch} = 1.2 nm and **(b)** T_{ch} = 2 nm and multiple S/D metals. In 1.2 nm In_2O_3 transistors, all contact metals demonstrate positive Φ_{SB}. On the other hand, for 2 nm In_2O_3 transistors, all contact metals demonstrate negative Φ_{SB}.

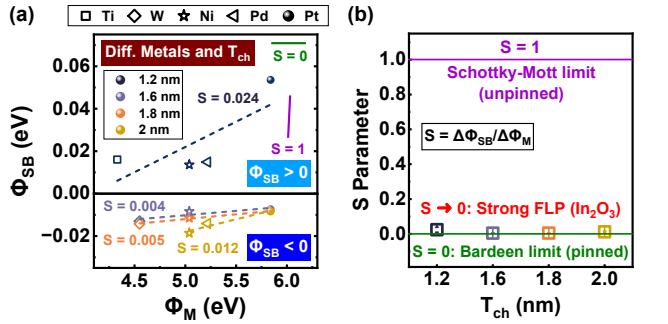

Fig. 14. (a) Relation between Φ_{SB} and Φ_M from In_2O_3 FETs with T_{ch} = 1.2 – 2 nm. S parameters can be extracted from the slope of the dash linear fitting lines. **(b)** S parameter as a function of T_{ch}. S = 1 (Schottky-Mott limit) means Φ_{SB} is unpinned (as described in **Fig. 12 (a)**). S = 0 (Bardeen limit) means Φ_{SB} is pinned at a certain value (like **Fig. 12 (c)**).

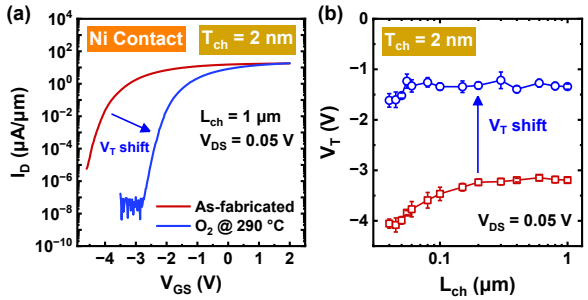

Fig. 15. (a) Transfer characteristics of In_2O_3 FETs with Ni as S/D contact, T_{ch} = 2 nm, and L_{ch} = 1 μm after 290 °C O_2 annealing for 10 minutes. **(b)** Linearly extrapolated V_T as a function of L_{ch}. O_2 annealing can shift V_T positively.

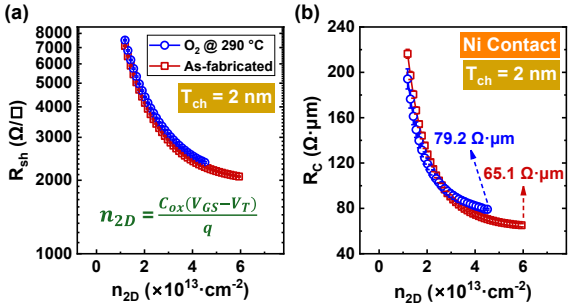

Fig. 16. O_2 annealing effect on **(a)** R_{sh} and **(b)** R_C extracted from TLM at room temperature (RT) as a function of carrier density (n_{2D}) in 2 nm In_2O_3 FETs with Ni contact. O_2 annealing devices still maintain good R_C of 79.2 Ω·μm at RT. Lower R_C of 23.4 Ω·μm can be achieved at lower temperature of 10 K [6-7].

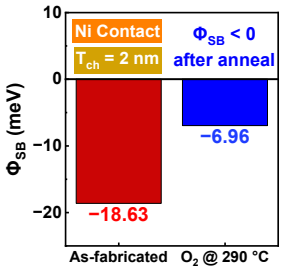

Fig. 17. Extracted Φ_{SB} from In_2O_3 FETs with Ni contact, T_{ch} = 2 nm, and L_{ch} = 1 μm before and after O_2 annealing. A negative Φ_{SB} can still be preserved after annealing.

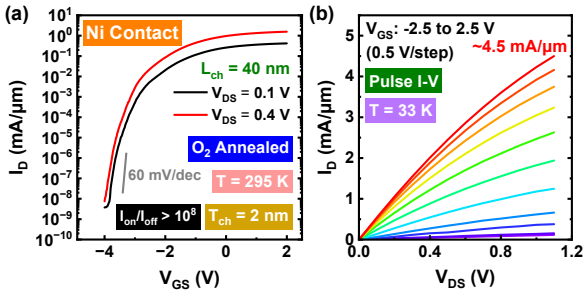

Fig. 18. (a) Transfer characteristics of a L_{ch} = 40 nm In_2O_3 FET with Ni contact after O_2 annealing. **(b)** Pulse I–V output characteristics of the device at 33 K with I_{max} ~ 4.5 mA/μm. Pulse I–V and low-temperature measurements can suppress the self-heating effect in In_2O_3 devices, which enables us to study the intrinsic performance of these devices [3, 6, 7].

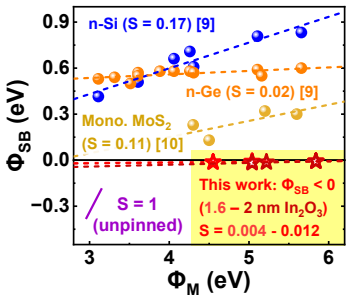

Fig. 19. Benchmark of reported FLP studies on n-Si [9], n-Ge [9], monolayer MoS_2 [10], and ultrathin In_2O_3 (this work: T_{ch} = 1.6 – 2 nm) with their S parameters. This work presents the first FLP study on ultrathin In_2O_3 FETs.